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Invention: ***"Plating Method and Apparatus that Creates a Differential Between Additive Disposed on a Top Surface and a Cavity Surface of a Workpiece Using an Indirect External Influence"***

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SPECIFICATION

**PLATING METHOD AND APPARATUS THAT CREATES A DIFFERENTIAL
BETWEEN ADDITIVE DISPOSED ON A TOP SURFACE AND A CAVITY
SURFACE OF A WORKPIECE USING AN INDIRECT EXTERNAL
INFLUENCE**

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This application is a continuation-in-part of Appln No. 09/740,701 filed in the U.S.
Patent & Trademark office on December 18, 2000 entitled "PLATING METHOD AND
APPARATUS THAT CREATES A DIFFERENTIAL BETWEEN ADDITIVE
10 DISPOSED ON A TOP SURFACE AND A CAVITY SURFACE OF A WORKPIECE
USING AN EXTERNAL INFLUENCE," which is based on priority application
60/224,739 filed August 10, 2000.

FIELD OF THE INVENTION

The present invention relates generally to a semiconductor plating method and
15 apparatus. More particularly, the present invention is directed to a method and apparatus
that creates a differential between additive adsorbed on a top surface of a workpiece and
additive adsorbed within a cavity portion of the workpiece using an indirect external
influence to enhance plating of a conductive material in the cavity portion of the
workpiece.

20 **BACKGROUND OF THE INVENTION**

There are many steps required in manufacturing multi-level integrated circuits
(IC). Such steps include depositing conductive and insulator materials on a
semiconductor wafer or substrate followed by full or partial removal of these materials
using photo-resist patterning, etching, and the like. After photolithography, patterning
25 and etching steps, the resulting surface is generally non-planar as it contains many

cavities or features such as vias, lines, trenches, channels, bond-pads, and the like that come in a wide variety of dimensions and shapes. These features are typically filled with a highly conductive metallic material before additional processing steps such as etching and/or chemical mechanical polishing (CMP) is/are performed. Accordingly, a low resistance interconnection structure is formed between the various levels/sections of the IC after completing these deposition and removal steps multiple times.

Copper (Cu) is quickly becoming the preferred material for interconnections in ICs because of its low electrical resistivity and high resistance to electro-migration. Electrodeposition is one of the most popular methods for depositing Cu into the features on the substrate surface.

As can be expected, there are many different designs of Cu plating systems that have been used in this industry. For example, U.S. Patent No. 5,516,412 issued on May 14, 1996, to Andricacos et al. discloses a vertical paddle plating cell that is designed to electrodeposit a film on a flat article. Next, U.S. Patent No. 5,985,123 issued on Nov. 16, 1999, to Koon discloses yet another vertical electroplating apparatus, which purports to overcome the non-uniform deposition problems associated with varying substrate sizes. Further, U.S. Patent No. 5,853,559 issued on Dec. 29, 1998, to Tamaki et al. discloses an electroplating apparatus that minimizes waste of the plating electrolyte and accomplishes high recovery of the electrolyte.

During the Cu electrodeposition process, specially formulated plating solutions or electrolytes are used. These solutions or electrolytes contain ionic species of Cu and additives to control the texture, morphology, and the plating behavior of the deposited material. Additives are needed to make the deposited layers smooth and somewhat shiny.

There are many types of Cu plating solution formulations, some of which are commercially available. One such formulation includes Cu-sulfate (CuSO_4) as the copper source (see James Kelly et al., Journal of The Electrochemical Society, Vol. 146, pages 2540-2545, (1999)) and includes water, sulfuric acid (H_2SO_4), and a small amount of chloride ions. As is well known, other chemicals can be added to the Cu plating solution to achieve desired properties of the deposited material.

The additives in the Cu plating solution can be classified under several categories such as suppressors, levelers, brighteners, grain refiners, wetting agents, stress-reducing agents, accelerators, etc. In many instances, different classifications are often used to describe similar functions of these additives. Today, solutions used in electronic applications, particularly in manufacturing ICs, contain simpler additives consisting of two-component packages (e.g., see Robert Mikkola and Linlin Chen, "Investigation of the Roles of the Additive Components for Second Generation Copper Electroplating Chemistries used for Advanced Interconnect Metallization", Proceedings of the International Interconnect Technology Conference, pages 117-119, June 5-7, 2000). These formulations are generically known as suppressors and accelerators. Some recently introduced packages also include a third component called levelers.

Suppressors are typically polymers formulated from polyethylene glycol-PEG or polypropylene glycol-PPG and are believed to attach themselves to the substrate surface at high current density regions, thereby forming a high resistance film, increasing polarization there and suppressing the current density and therefore the amount of material deposited thereon. Accelerators are typically organic disulfides or other compounds that enhance Cu deposition on portions of the substrate surface where they

are adsorbed. The interplay between these two additives and possibly the chloride ions determines the nature of the Cu deposit.

The following figures are used to more fully describe the conventional electrodeposition method and apparatus. Fig. 1 illustrates a perspective view of a cross-section of a test-substrate 3 having an insulator 2 formed thereon. Using conventional etching techniques, features such as a row of small vias 4a and a wide trench 4b are formed on the insulator 2 and the substrate 3. In this example, the vias 4a are narrow and deep; in other words, they have high aspect ratios (i.e., their depth to width ratio is large). Typically, the widths of the vias 4a are sub-micron. The trench 4b, on the other hand, is typically wide and has a small aspect ratio. In other words, the width of the trench 4b may be five to fifty times or more greater than its depth.

Figs. 2a -2c illustrate a conventional method for filling the features with Cu. Fig. 2a illustrates a cross sectional view of the substrate 3 in Fig. 1 having various layers disposed thereon. For example, this figure illustrates the substrate 3 and the insulator 2 having deposited thereon a barrier/glue or adhesion layer 5 and a seed layer 6. The barrier layer 5 may be tantalum, nitrides of tantalum, titanium, tungsten, or TiW, etc., or combinations of any other materials that are commonly used in this field. The barrier layer 5 is generally deposited using any of the various sputtering methods, by chemical vapor deposition (CVD), or by electroless plating methods. Thereafter, the seed layer 6 is deposited over the barrier layer 5. The seed layer 6 material may be copper or copper substitutes and may be deposited on the barrier layer 5 using various sputtering methods, CVD, or electroless deposition or combinations thereof.

In Fig. 2b, after depositing the seed layer 6, a conductive material 7 (e.g., copper layer) is generally electrodeposited thereon from a suitable acidic or non-acidic plating

bath or bath formulation. During this step, an electrical contact is made to the Cu seed layer 6 and/or the barrier layer 5 so that a cathodic (negative) voltage can be applied thereto with respect to an anode (not shown). Thereafter, the Cu material 7 is electrodeposited over the substrate surface using the specially formulated plating solutions, as discussed above. By adjusting the amounts of the additives, such as the chloride ions, suppressor/inhibitor, and the accelerator, it is possible to obtain bottom-up Cu film growth in the small features.

The Cu material 7 completely fills the via 4a and is generally uniform in the large trench 4b, but does not completely fill the trench 4b because the additives that are used are not operative in large features. For example, it is believed that the bottom up deposition into the via 4a occurs because the suppressor/inhibitor molecules attach themselves to the top of the via 4a to suppress the material growth thereabouts. These molecules can not effectively diffuse to the bottom surface of the via 4a through the narrow opening. Preferential adsorption of the accelerator on the bottom surface of the via 4a, therefore, results in faster growth in that region, resulting in bottom-up growth and the Cu deposit profile as shown in Fig. 2b. Without the appropriate additives, Cu can grow on the vertical walls as well as the bottom surface of the via 4a at the same rate, thereby causing defects such as seams and/or voids, as well known in the industry.

Adsorption characteristics of the suppressor and accelerator additives on the bottom surface of the large trench 4b is not expected to be any different than the adsorption characteristics on the top surface of the field regions 8 of the substrate. Therefore, the Cu thickness t_1 at the bottom surface of the trench 4b is about the same as the Cu thickness t_2 over the field regions 8.

As can be expected, to completely fill the trench 4b with the Cu material 7, further

plating is required. Fig. 2c illustrates the resulting structure after additional Cu plating. In this case, the Cu thickness t_3 over the field regions 8 is relatively large and there is a step s_1 from the field regions 8 to the top of the Cu material 7 in the trench 4b. For IC applications, the Cu material 7 needs to be subjected to CMP or other material removal process so that the Cu material 7 as well as the barrier layer 5 in the field regions 8 are removed, thereby leaving the Cu material 7 only within the features. These removal processes are known to be quite costly.

Thus far, much attention has been focused on the development of Cu plating chemistries and plating techniques that yield bottom-up filling of small features on substrates. This is necessary because, as mentioned above, lack of bottom-up filling can cause defects in the small features. As part of these development efforts, it was discovered that the filling behavior of the small features could be affected not only by the solution chemistry, but also by the type of the power supply used for electrodeposition.

Recent studies suggest that it might be preferable to use pulse or pulse-reverse plating methods to deposit defect free Cu into the small vias (e.g., U.S. Patent 5,972,192 issued to Dubin et al. on October 26, 1999, and Gandikota et al. "Extension of Copper Plating to 0.13 μm Nodes by Pulse-Modulated Plating", Proceedings of the International Interconnect Technology Conference, pages 239-241, June 5-7, 2000). In the pulse-reverse plating process, a cathodic voltage pulse rather than a cathodic DC voltage is applied to the substrate surface. After a short period of plating during the cathodic pulse, the polarity of the voltage is reversed for a brief period causing electrochemical etching from the deposited material. Plating and etching cycles are then repeated until the small features are filled with high quality Cu. A recent study (e.g., C.H. Hsieh et al., "Film Properties and Surface Profile after Gap Fill of Electrochemically Deposited Cu Films by

DC and Pulse Reverse Processes”, Proceedings of the International Interconnect Technology Conference, pages 182-184, June 5-7, 2000), shows that the filling of the vias is controlled mainly by the additive diffusion when the DC process is used, whereas it is mainly controlled by additive adsorption when a pulse-reverse process is used.

5 As described above, there is much interest in the semiconductor industry in filling the various features on semiconductor wafers with Cu in an economical way using the electro-deposition technique. Both DC and pulsed power supplies have been used in the deposition of these Cu films. Filling properties of Cu into small features were found to be a strong function of the type of the power supply used. Although the exact roles of the plating solution additives and their interaction with the applied voltage waveforms are
10 not well understood, it is clear that the kinetics of the additive adsorption and diffusion processes influence the way metals deposit on non-planar substrate surfaces.

As mentioned above, special bath formulations and pulse plating processes have been developed to obtain bottom-up filling of the small features. However, these
15 techniques have not been found effective in filling the large features. In large features, the additives can freely diffuse in and out of them. The use of standard pulse plating techniques in conjunction with the commonly used additive systems containing chloride ions, accelerators and suppressors/inhibitors do not yield accelerated growth from the bottom surface of the features where the width of the feature is considerably larger than
20 its depth. The growth of Cu in such features is conformal and the film thickness deposited on the bottom surface of the large features is approximately the same as that deposited on the field regions.

Methods and apparatus to achieve accelerated bottom-up plating in small as well as large features on a substrate would be invaluable in terms of process efficiency and

cost since such a process would yield a Cu deposit that is generally planar as illustrated in Fig. 3. The Cu thickness t_5 over the field regions 8 in this example is smaller than the traditional case as shown in Fig. 2c, and the step height s_2 would also be much smaller. Removal of the thinner Cu layer in Fig. 3 by CMP or other methods would be easier,
5 providing important cost savings.

Others have previously recognized attractive features of a plated Cu structure such as the one shown in Fig. 3. For example, in a PCT application ("Electroplated Interconnection Structures on Integrated Circuit Chips", WO 98/27585, June 25, 1998) researchers from International Business Machines Corporation state that the plating
10 processes described therein produce super-filling of only the sub-micron size cavities when plating was carried out in a conventional plating cell. However, it also states that a further benefit could be realized when a cup plating cell is used as described in U.S. Patent No. 4,339,319 issued on July 13, 1982, to Aigo. In addition, when the substrate surface was held in contact with the meniscus of the electrolyte during plating in a cup
15 plating cell, cavities of greatly different widths could be filled rapidly at the same rate yielding a structure similar to that shown in Fig. 3. The PCT application also mentions that superior performance of the meniscus plating approach was due to the higher concentration of the surface active additive molecules at the air-liquid interface.

In the recently issued U.S. Patent No 6,176,992 B1, entitled "Method and
20 apparatus for electrochemical mechanical deposition", commonly owned by the assignee of the present invention, a technique is disclosed that achieves deposition of the conductive material into the cavities on the substrate surface while minimizing deposition on the field regions by polishing the field regions with a pad as the conductive material is deposited. The plating electrolyte in this application is supplied to the small gap between

the pad and the substrate surface through a porous pad or through asparities in the pad.

Fig. 4 shows a schematic depiction of an electrochemical mechanical deposition apparatus that can be used for planar or near-planar Cu deposition on a semiconductor wafer. A carrier head 10 holds a semiconductor wafer 16 and provides an electrical lead 17 connected to the conductive portion of the wafer 16. The head 10 can be rotated clockwise or counter-clockwise about a first axis 10b and can be moved in x, y, and z directions. A pad 18 is provided on top of an anode assembly 19, which pad 18 faces the wafer 16. An electrolyte 20 containing the plating material is applied to the wafer 16 surface using the anode assembly 19. The electrolyte 20 can be flowed through the holes/openings in the pad 18, which makes physical contact with the wafer 16 surface. The electrolyte 20 then flows in the narrow gap between the wafer 16 and the pad 18, eventually flowing over the edges of the pad 18 into a chamber 22 to be re-circulated (not shown) after cleaning/filtering/refurbishing. A second electrical lead 24 is connected to the anode assembly 19. Any other known method for providing the electric potentials to the anode assembly 19 and cathode wafer 16 can be used herein.

The anode assembly 19 can also be rotated around a second axis 10c at controlled speeds in both the clockwise and counter-clockwise directions. It is also understood that axes 10b and 10c are substantially parallel to each other. The gap between the wafer 16 and the pad 18 is adjustable by moving the carrier head 10 in the z direction. When the wafer 16 surface and the pad 18 are in contact, the pressure that is exerted on the two surfaces can also be adjusted. The co-pending U.S. Application Serial No. 09/511,278, entitled "Pad Designs and Structures for a Versatile Materials Processing Apparatus", filed February 23, 2000, describes various shapes and forms of the holes in the pad 8, through which the electrolyte flows to the wafer surface.

During operation, a potential is applied between the electrical lead 17 to the wafer 16 and the electrical lead 24 to the anode assembly 19, making the wafer 16 surface more negative than the anode assembly 19. The electrolyte 20 can be introduced to the pad 18 from a reservoir (not shown) located in proximity to the anode assembly 19. The anode assembly 19 can have an in-channel and holes that are made therein, which together provide a path for the electrolyte 20 to be fed to the gap between the pad 18 and the wafer 16.

Under applied potential, Cu plates out of the electrolyte 20 onto the wafer 16 surface. The moving pad 18 that is pushed against the wafer 16 surface at a controlled pressure minimizes accumulation of Cu over certain portions of the wafer 16 surface by polishing the same.

The pad 18 is preferably nonconductive, hard, porous, or perforated type material so that an electric field can pass through it, while preventing shorting between the anode assembly 19 and the cathode wafer 16. The spacing or gap between the pad 18 and the cathode wafer 16 may range from less than 1 micron up to 2 millimeter. The diameter or cross sectional length of the pad 18 and the wafer 16 may range from about 5 millimeter to over 300 millimeter. The larger the wafer 16 diameter, the larger the pad 18 diameter. While many of the above-described processes are very advantageous, further improvements are nonetheless desirable.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method and apparatus that plates a conductive material on a substrate surface.

It is another object of the present invention to provide a method and apparatus that

plates a conductive material in both small and large features of a substrate surface with greater efficiency, cost-savings, and superior quality than prior art methods and apparatus. It is yet another object of the present invention to provide a method and apparatus that plates a conductive material in small and large features while electrical power is locally pulsed on the substrate surface.

It is a further object of the present invention to provide a method and apparatus that removes additive(s) that has or have been previously adsorbed onto the top surface portion of a workpiece in order to enhance the plating of a conductive material on a cavity feature surface portion of the workpiece that did not have previously adsorbed additive removed.

It is yet another object of the present invention to create a differential between additive adsorbed on a top surface of a workpiece and additive adsorbed within a cavity portion of the workpiece to enhance plating of a conductive material in the cavity portion of the workpiece.

It is another object of the present invention to create a differential between additive adsorbed on a top surface of a workpiece and additive adsorbed within a cavity portion of the workpiece so that the electrical resistance on the top surface is higher than electrical resistance of the surfaces within the cavity to result in enhanced plating into the cavity.

It is a further object of the present invention to cyclically remove an additive that has been previously adsorbed onto the top surface portion of a workpiece using a mask that is disposed spaced relation to the workpiece and then to plate a conductive material on a cavity feature surface portion of the workpiece with the mask no longer contacting any point on the workpiece so that plating within the cavity portion occurs at a higher rate

than any plating on the top surface of the workpiece.

It is a further object of the present invention to remove an additive that has been previously adsorbed onto the top surface portion of a workpiece using a mask that is disposed in spaced relation to the workpiece during a period when no power is applied to the workpiece surface and then to plate a conductive material on the workpiece.

It is a further object of the present invention to create a differential between additive adsorbed on a top surface of a workpiece and additive adsorbed within a cavity portion of the workpiece to enhance plating of a conductive material in the cavity portion of the workpiece using an external influence that does not directly physically contact the workpiece.

The above objects of the invention, among others, taken alone or in combination, are achieved by the present invention, which provides apparatus for, and methods of, plating a conductive material on the surface of a workpiece.

In one aspect of the method, an electrolyte solution with at least one additive disposed therein is applied over the workpiece, such that the additive becomes adsorbed onto the top portion and the cavity portion of the workpiece. An external influence is applied using a mask that is in spaced relation that is proximate to but does not contact the top surface of the workpiece while the workpiece and mask move relative to each other so that the additive adsorbed onto the top surface is removed or otherwise changed with respect to the additive on the cavity surface of the workpiece. Plating of the conductive material subsequently takes place before the additive fully re-adsorbs onto the top portion, thereby causing greater plating of the cavity portion relative to the top portion.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become apparent and more readily appreciated from the following detailed description of the presently preferred exemplary embodiments of the invention taken in conjunction with the accompanying drawings, of which:

Fig. 1 illustrates a perspective view of a cross section of a substrate having an insulator layer and various features formed thereon;

Figs. 2a-2c illustrate cross sectional views of a conventional method for depositing a conductive material on the substrate of Fig. 1;

Fig. 3 illustrates a cross sectional view of a substrate having a conductive material deposited thereon in accordance with another conventional method;

Fig. 4 illustrates an example of an electrochemical mechanical deposition apparatus;

Fig. 5 illustrates a conventional plating cell having an anode, cathode, and electrolyte disposed therein;

Fig. 6 illustrates a partial view of an apparatus in accordance with the preferred embodiment of the present invention;

Figs. 7a-7d illustrate a mask pulsed plating method in accordance with the preferred embodiment of the present invention; and

Fig. 7e illustrates a graph corresponding to Figs. 7a-7d in accordance with the preferred embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will now be described with reference to the following figures. The inventors of the present invention have found that by mask-pulse plating the conductive material on the substrate surface, a more desirable and high quality conductive material can be deposited in the various features therein.

The present invention can be used with any substrate such as a semiconductor wafer, flat panel, magnetic film head, packaging substrate, and the like. Further, specific processing parameters such as time, pressure, mask designs, and the like are provided herein, which specific parameters are intended to be explanatory rather than limiting.

The plating method described herein is called "mask-pulsed" plating. The present invention describes a method and apparatus for mask-pulse plating the conductive material onto the substrate by creating an external influence that removes or changes additive adsorbed onto the top surface of the substrate with respect to the additive on the cavity surface of the substrate. This external influence can be created, as described in the preferred embodiment, by intermittently moving the a mask disposed in spaced relation that is proximate to but does not contact the substrate surface and applying power between an anode and the substrate, the mask being positioned in between the anode and the substrate. Furthermore, the present invention is directed to novel plating method and apparatus that provide enhanced electrodeposition of conductive materials into the various features on the substrate surface.

Fig. 5 illustrates a plating cell 30 having therein an anode 31, a cathode 32, and an electrolyte 33. It should be noted that the plating cell 30 is a conventional cell and the exact geometry of the plating cell used in the present invention can vary. The electrolyte 33 is in contact with the top surface of the cathode 32. The cathode 32 in the examples

provided herein is a wafer (substrate) having various features on its top surface. When a DC or pulsed voltage is applied between the wafer 32 and the anode 31, Cu from the electrolyte 33 is deposited on the wafer 32 as described above. The differences between the DC or pulsed power determines the quality of the Cu that is filled in the small features.

Fig. 6 illustrates a preferred embodiment of the present invention. In the present invention, a mask 40 is positioned in close proximity to the cathode wafer 32, which is typically less than .75 mm and preferably in the range of 0.1 to 0.5 mm, and the relative movement is preferably at speeds between the range of 1 to 100 cm/s. The mask 40 can include an opening 42 through which the electrolyte 33 can travel, or can have a configuration without openings, but allows for the creation of a differential between additives on a top surface of the substrate and cavity portions of the substrate, as described hereinafter. The mask is typically flat, and can also have a textured surface, such that at a microscale level it is rough. For ease of understanding and explanation, Fig. 6 does not illustrate the electrical connections, the anode, and the plating cell containing the electrolyte 33. When an appropriate voltage is applied between the cathode wafer 32 and the anode, the opening 42 allows the Cu from the electrolyte 33 to be plated onto the surface of the substrate 32 below the opening 42 in an amount greater than plating that may occur in areas not below an opening.

Figs. 7a-7d illustrate a mask pulsed plating method in accordance with the preferred embodiment of the present invention in which the mask 40 contains a single opening 42. The mask 40 is moved to the left with respect to the cathode wafer 32 (or alternatively, the wafer 32 may be moved to the right, or both the mask 40 and the wafer 32 may be moved relative to each other). In Fig. 7a, at time $t=t_1$, a section 45 on the

wafer 32 surface is positioned under the electrically insulating mask 40. Accordingly, the plating current at the section 45 at $t=t_1$ is very small or near zero as depicted in the graph of Fig. 7e. Fig. 7e illustrates a graph depicting the deposition/plating current in relation to time at the section 45.

5 In Fig. 7b, as the mask 40 and/or the wafer 32 is moved such that the opening 42 is above the section 45, the plating current at the section 45 at time $t=t_2$ increases sharply as the opening 42 aligns with the section 45. In Fig. 7c, the high current remains steady until $t=t_3$. Thereafter, when the section 45 is again positioned underneath the non-opened portion of the mask 40 as shown in Fig. 7d, the current density is again very small or near zero.

10 Referring back to Fig. 7e, the time interval Δt (time between t_2 and t_3) is a function of the speed of the mask 40 as well as the size of the opening 42. In addition, Δt will be a small value if the mask 40 is moved rapidly in relation to the wafer 32. Also, if there are multiple openings in the mask 40 or if the movement of the mask 40 is back and forth, 15 then the corresponding current vs. time plots would consist of multiple pulses. By controlling the size of the opening(s) on the mask 40 and the relative speed of the substrate and the mask, the shape, duration and repetition rate of the current pulses at any section on the substrate can be controlled. If the current mask-pulsed plating method is used with simple metal deposition electrolytes with no additives (i.e., inhibitors and 20 accelerators), it would not be expected to be much different than conventional plating. This is because the size of the openings 42 in the mask 40 is much larger than the feature size on the wafer 32 surface. Therefore, when a section is exposed through the opening 42, , regular plating would commence. However, if additives are added that influence polarization, then the mask-pulsed plating method can offer advantages that is not

existent in conventional pulsed plating techniques.

For example, consider a Cu plating bath containing conventional solutions/chemicals (Cu sulfate, water, sulfuric acid and chloride ions) and an additive A. The additive A enhances deposition when it is adsorbed on the wafer surface. When this electrolyte is used in a conventional plating cell such as the one depicted in Fig. 5, the entire surface of the wafer 32 will be exposed to the electrolyte and the additive A. The field regions on the wafer surface, as well as the bottom surface of the large features would likewise adsorb the additive A and plating begins on these surfaces at comparable rates.

If, however, the mask-pulsed plating technique is used with the same electrolyte, the external influence on the top surface of the wafer 32 caused by, for example, the mask 40 that is disposed in proximity to the wafer 32, would clear away the additive A from the field regions. Both the small and large features, however, will still contain the adsorbed additive A since these features are further removed from the external influence than the top surface of the wafer 32. When a section of the wafer is suddenly exposed to the opening in the pad, the bottom and side surfaces of the features with the previously adsorbed additive A would immediately start plating at a higher rate than the field regions. If the time period Δt is less than the adsorption period required for the additive A to attach itself to the substrate surface, the applied plating current preferentially flows through the features to be filled, thereby yielding an enhanced deposition rate within the features in relation to the deposition rate on the field regions.

The mask-pulsed plating method of the present invention utilizes the differences between response times of various additives to achieve enhanced plating into the various features of the substrate surface. The mechanism involves "sweeping" of the top surface

of the substrate (field regions) by the mask, which produces much less agitation of the electrolyte disposed inside the features than on the top surface of the wafer 32, and thereby relatively sweeps additives disposed on the top surface of the wafer 32 more than additives disposed within cavity portions. The sweeping on the field regions establishes a differential between the concentration of the adsorbed species in those regions that are swept away and the regions that are within the features. When the surface is then suddenly exposed to the opening in the mask and the electric field, the features with the adsorbed species attracts most of the plating current from the field regions.

This present method works equally well using multiple additives. For example, if the plating solution contains an inhibitor B and an accelerator C with the adsorption kinetics of the inhibitor being much faster than that of accelerator, the following mechanism can be used by the mask-pulsed plating method described herein. Both the inhibitor B and the accelerator C would be partially or wholly swept off the field regions of the substrate by the motion of the mask. However, both species would still be present in the features. When the substrate is exposed to the opening in the mask and the electric field, the inhibitor B would readily adsorb onto the field regions introducing a high resistance path for the plating current. The accelerator C, which is already present within the features, compensates for the action of the inhibitor in those regions and the current can easily flow through these features. Therefore, until the accelerator C is properly adsorbed onto the field regions, the film growth rate within the features will be higher.

This same result can also be expected from yet another chemistry where an inhibitor D has the property of strong adsorption and the accelerator E is weakly bonded to the field regions. In this case, the motion of the mask can readily remove the weakly bonded accelerator E from the field regions whereas, the accelerator E remains attached

to the surfaces within the features. Upon exposure to the opening in the mask and electric field, the plating current flows through the features preferentially until the accelerator E begins to get adsorbed again onto the field regions.

It should be noted that the above descriptions are just some examples of the mechanisms involved in the present invention and are not meant to be limiting. The present invention utilizes differences between adsorption/de-sorption kinetic of various electrolyte additives. The present invention accomplishes this by applying a solution and power suddenly and simultaneously to a specific section of the substrate surface that has been previously cleared off, partially or wholly, of one or more of the additive species. In this regard, inhibitors/suppressors are additives that inhibit deposition on surfaces they get attached/adsorbed. They do this by increasing polarization there. Increased polarization is due to increased resistance. Accelerators are additives that enhance deposition on surfaces they get attached/adsorbed. There are other additives that may be called other names such as brighteners, levelers etc. However, irrespective what such additives are called, they either have inhibitor or accelerator characteristics. Therefore, suppressors can be viewed as additives with deposition inhibiting characteristics whereas accelerators can be viewed as additives with deposition enhancing characteristics, irrespective of the trade names or other identifying names associated with such additives.

It is also noted that other additives, whether surface active or not, can also be included in the plating solution. In fact, addition of certain chemicals can influence the adsorption or desorption of the accelerators and/or suppressors in a beneficial manner. For example, in a case where the accelerator is being removed from the top surface, addition of a chemical in the solution chemistry that loosens the bond between the top surface and the accelerator can be beneficial because the mask can remove the loosely

bound additive more easily. An example of one such group of chemicals is alcohol.

The geometry of the plating system shown in Fig. 6 is quite simplistic. There are many possible designs that can be used to practice this invention. Some aspects of the present invention are as follows.

5 (1) The mask may be flat when using a wafer that is also flat. The mask is preferably made of an insulating rigid material and the surface facing the wafer may be hard and even contain abrasives to help "sweep" away the additives more efficiently.

(2) There may be a relative movement between the wafer and the mask. The wafer, mask, or both may be moved in linear or orbital manner or combination thereof.

10 (3) The size of the opening(s) in the mask and the speed of the relative motion between the mask and the wafer may be such that any section on the wafer will have plating occur while a differential exists. This differential time interval can be adjusted with respect to the adsorption characteristics of the additives being used.

15 The power supply used in the present invention may be pulsed or DC power supply, but preferably it is a DC power supply. The power supply can be used in the current controlled or voltage controlled mode, i.e., it either keeps the applied current constant or applied voltage constant. For the case of using a current controlled mode, it is preferable that the size of the opening(s) in the mask be large enough to cover portions of the field regions as well as portions of the features simultaneously. In other words, when
20 the wafer surface is exposed to the plating current through the opening(s), there should not be just the field regions that are exposed to the electrolyte at any given time. For example, if the opening is very small or the number of features on the wafer surface is low (low density features), the field regions are exposed to the plating current. In this case, since the power supply pushes through a fixed current, all the current would flow

through the field regions and the Cu will be plated on the field region without discrimination. But if both field regions and features are exposed simultaneously, then the current would preferentially flow through the features and more Cu would be plated into the features and less on the field regions. This situation can be assured by increasing the number of openings in the mask so that there are always portions of the both regions (field and feature) exposed to the plating current through some of the openings simultaneously.

If a constant voltage power supply is used, then the current automatically adjusts itself depending upon the resistance on the wafer surface. Therefore, if the mask hole exposes only the field regions of the wafer, less current is supplied to that surface and the plating amount is smaller. When features are exposed to the mask opening, more current flows into the feature and thus preferential plating takes place into the features. Therefore, it is more appropriate to use voltage controlled mode of the power supply if wafers with low feature density is coated and/or the number of holes in the mask is limited.

This invention can be used to fill both small and large features. However, a serial process can also be utilized. In that approach, there are two processing steps. During the first step the mask is pulled away from the wafer surface allowing substantial amount of plating solution between the mask and the wafer surface. In this position, the system acts just like a traditional plating cell. With the help of the additives in the plating solution, the small features are filled during this step and the situation as shown in Fig. 2b occurs. During this first step, the mask and the wafer are moved with respect to each other for uniform deposition. Then the mask is brought in proximity to the wafer. Mask-pulsed plating then commences to preferentially fill the larger features as described earlier.

Along with using copper and its alloys as the conductive material, other conductive materials such as copper alloys, iron, nickel, chromium, indium, lead, tin, lead-tin alloys, nonleaded solderable alloys, silver, zinc, cadmium, ruthenium, their respective alloys may be used in the present invention. The present invention is especially suited for the fabrication of high performance and highly reliable chip interconnect, packaging, magnetic, flat panel and opto-electronic applications. In another embodiment of the present invention, a mask as described above is used to come in close proximity to the workpiece surface when creating the external influence. An external influence is thus applied using the mask so that the additive adsorbed onto the top surface is removed or otherwise changed with respect to the additive on the cavity surface of the workpiece. The mask can be applied in close proximity to the wafer as described above, typically for a period of 1 to 5 seconds or until a differential is created between the resistance of the top surface and the cavity surface resulting from a differential in additives. After creating the differential between in the additives disposed on the top surface portion of the workpiece and the cavity surface portion of the workpiece, as described above, the mask is moved further away from the workpiece surface, preferably at least 0.1 cm, so that plating can occur thereafter. As long as the differential in additives remains, plating can then occur. The plating period is directly related to the adsorption rates of the additives. During this time, due to the differential, plating will occur more within features on than on the surface of the workpiece. Since the electrolyte is disposed over the entire workpiece surface, this also assists in lowering the current density and improving thickness uniformity of the plated layer. When the mask is moved further away from the workpiece, electric field lines can bend in the region between the mask and the surface of the workpiece yielding more uniform film.

Once a sufficient differential no longer exists, the mask can again moved in proximity to the workpiece surface and create the external influence, as described above. This process can cyclically repeat until plating of the conductive material to the desired thickness is achieved.

5 In another aspect of this embodiment, plating can be initiated while the mask is in close proximity to the top portion of the workpiece and the workpiece and mask move relative to each other, and then plating can continue while the mask is no longer in close proximity to the top portion of the workpiece while the sufficient differential exists.

Since plating occurs both when there is close proximity between the mask and the workpiece, as well as when there is not, this can provide faster processing. It should be noted that additives should be carefully chosen for this application. Specifically, the additive species that need to be removed by the influence without physical contact should have weak adsorption characteristics so that they can be removed without direct contact between the mask and the wafer.

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15 In another embodiment, it is recognized that the plating current can affect adsorption characteristics of additives. For some additives adsorption is stronger on surfaces through which an electrical current passes. In such cases, adsorbing species may easily be removed from the surface they were attached to, after power is cut off or reduced from that surface (current passing through is cut off or reduced). Loosely bound additives can then be removed easily by the mask. In the cavities, although loosely bound, additives can stay more easily because they do not get influenced by the external influence.

20 In the previous descriptions, numerous specific details are set forth, such as specific materials, mask designs, pressures, chemicals, processes, etc., to provide a

thorough understanding of the present invention. However, as one having ordinary skill in the art would recognize, the present invention can be practiced without resorting to the details specifically set forth.

Although various preferred embodiments have been described in detail above,
5 those skilled in the art will readily appreciate that many modifications of the exemplary embodiment are possible without materially departing from the novel teachings and advantages of this invention. For example, the distance that the mask can be moved away from the wafer and still be in close proximity, and thereby exert an external influence can increase, or a force that is obtained from something other than a mask can be used, such
10 as, for example, a directed jet of an electrolyte that is used to agitate the additives on the top surface of the wafer. Accordingly, the invention is properly construed by the claims provided below.

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